

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A node controller for a data storage system having at least one node for providing access to a data storage facility, the node controller distinct from a computer-memory complex of the node, the node controller providing overall control for transferring data through the node, wherein the node controller comprises a logic engine operable to perform a logic operation on data from at least one data source in the data storage system.
- Claim 2 (canceled).
3. (currently amended) The node controller of Claim [[2]] 1 wherein the at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory.
4. (currently amended) The node controller of Claim [[2]] 1 wherein the logic engine comprises an exclusive OR engine.
5. (currently amended) The node controller of Claim 1 comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying said at least one data source.
6. (original) The node controller of Claim 1 comprising a memory controller operable to interface with a cluster memory in the node.
7. (original) The node controller of Claim 1 wherein the node controller is implemented as an integrated circuit device.
8. (original) The node controller of Claim 1 comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus.
9. (original) A node controller for providing overall control for transferring data through a node of a data storage system, the node controller distinct from a computer-memory complex of the node, the node controller comprising:

a logic engine operable to perform a logic operation on data from at least one data source in the data storage system; and

a command queue coupled to the logic engine, the command queue operable to store a logic control block which can be processed by the logic engine.

10. (original) The node controller of Claim 9 wherein the at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory.
11. (original) The node controller of Claim 9 wherein the logic engine comprises an exclusive OR engine.
12. (original) The node controller of Claim 9 comprising a memory controller operable to interface with a cluster memory in the node.
13. (original) The node controller of Claim 9 wherein the node controller is implemented as an integrated circuit device.
14. (original) The node controller of Claim 9 comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus managed by the computer-memory complex.
15. (original) The node controller of Claim 9 wherein the node controller is operable to be programmed by the computer-memory complex.
16. (original) The node controller of Claim 9 comprising:
- a producer register operable to specify a first address of the command queue; and
 - a consumer register operable to specify a second address of the command queue.

Claim 17 (canceled).

18. (new) A node controller for transferring data through a node in a data storage system, the node controller comprising:
- a plurality of input/output interfaces for coupling to a plurality of buses, wherein the buses are coupled to a computer-memory complex of the node and each bus can be coupled to a plurality of devices;

a memory controller for coupling to (1) a memory and (2) a backplane, wherein the backplane can be coupled to a plurality of other node controllers in the data storage system;

a plurality of logic engines coupled to (1) the memory controller and (2) the backplane;

a plurality of command queues storing logic control blocks each defining (1) a logic operation to be performed by a logic engine, (2) a plurality of data sources for the logic operation, and (3) a data destination for a result of the logic operation;

wherein the logic engine performs the logic operation to a plurality of data from the plurality of data sources and writes the result of the logic operation to the data destination, each of the plurality of data sources being selected from the group consisting of one region in the memory and one of the devices, the data destination being selected from the group consisting of one region in the memory, one of the devices, and one of the other node controllers.

19. (new) The controller node of claim 18, wherein in a second type of data transfer, a data source writes a data into the memory and in response the logic engine copies the data to at least one data destination, the data source being selected from the group consisting of one of the devices and one of the other node controllers, the data destination being selected from the group consisting of one region in the memory, one of the devices, and one of the other node controllers.
20. (new) The controller node of claim 19, wherein each of the devices is selected from the group consisting of a host device and a data storage device.
21. (new) The controller node of claim 20, wherein each of the input/output interfaces comprises a peripheral component interconnect (PCI) controller and each of the buses comprises a PCI bus.
22. (new) The controller node of claim 21, wherein the computer-memory complex manages the PCI bus.
23. (new) The controller node of claim 22, wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

24. (new) The controller node of claim 18, wherein said burdening a computer-memory complex of the node comprises temporarily storing data being transferred through the node in the computer-memory complex.
25. (new) The controller node of claim 18, wherein the logic operation comprises an XOR operation.
26. (new) The controller node of claim 25, wherein the XOR operation is used to calculate a parity data for writing a full or a partial RAID stripe.
27. (new) The controller node of claim 25, wherein the XOR operation is used to reconstruct a lost data using a parity data.